EAST Browser - L12: (21) 11 and refresh | US 5923593 A | Tag: S | Doc: 20/21 | Format: KWIC

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Abstract Text - ABTX (1):

A multi-port DRAM cell structure that enables read, write and refresh accesses at each port of the DRAM cell. The DRAM cell includes a storage capacitor for storing a data value, and a plurality of ports for accessing the storage capacitor. Each port enables both read and write accesses to the storage capacitor. Each port can include a port access transistor, a port bitline and a port wordline. The port access transistor includes a gate electrode, a source and a drain. The source of the port access transistor is coupled to the storage capacitor, the drain of the port access transistor is coupled to the port bitline, and the gate electrode of the port access transistor is coupled to the port wordline. This cell architecture enables overlapping read and write accesses to be simultaneously performed at the various ports of the multi-port DRAM cell.

Brief Summary Text - BSTX (11):

Another limitation is that a refresh access can only be performed at one port of DRAM cells 200 and 300 (i.e., the write port). The charge stored in the storage capacitors of cells 200 and 300 can be depleted by leakage through the read and/or write access transistors. To compensate for this charge depletion, the storage capacitors must be periodically refreshed. A refresh access is performed by performing a read access followed by a write access.

Details | Text | Image | HTML | KWIC

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[75] Inventors: Fu-Chieh Hsu, Saratoga; Wingyu Leung, Cupertino, both of Calif.

[73] Assignee: Monolithic Systems, Inc., Sunnyvale, Calif.

[21] Appl. No.: 08/767,707

[22] Filed: Dec. 17, 1996

[51] Int. Cl.[6] G11C 7/00; G11C 8/00

[52] U.S. Cl. 365/189.04; 365/149; 365/230.05

[58] Field of Search 365/189.04, 149, 365/210, 230.05, 189.01

[56] References Cited

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5,355,335 10/1994 Katsuno 365/189.04

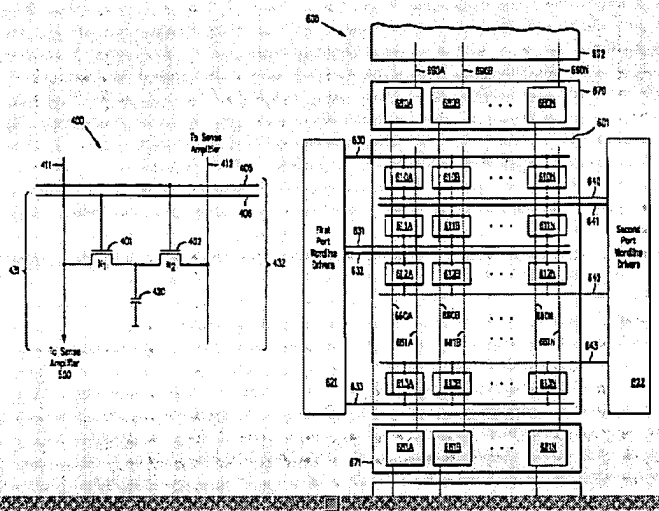
Primary Examiner—Son Mai

Attorney, Agent, or Firm—Skjerven, Morrill MacPherson, Franklin & Friel LLP; Norman R. Klivans

[57] ABSTRACT

A multi-port DRAM cell structure that enables read, write and refresh accesses at each port of the DRAM cell. The DRAM cell includes a storage capacitor for storing a data value, and a plurality of ports for accessing the storage capacitor. Each port enables both read and write accesses to the storage capacitor. Each port can include a port access transistor, a port bitline and a port wordline. The port access transistor includes a gate electrode, a source and a drain. The source of the port access transistor is coupled to the storage capacitor, the drain of the port access transistor is coupled to the port bitline, and the gate electrode of the port access transistor is coupled to the port wordline. This cell architecture enables overlapping read and write accesses to be simultaneously performed at the various ports of the multi-port DRAM cell.

15 Claims, 7 Drawing Sheets



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	Document ID	Kind Codes	Source	Issue Date	Pa
1	US 20030063517		US-PGPU	20030403	9
2	US 20030063515		US-PGPU	20030403	8
3	US 20020167845		US-PGPU	20021114	10
4	US 20020167837		US-PGPU	20021114	11
5	US 20020167836		US-PGPU	20021114	5
6	US 20020167834		US-PGPU	20021114	7
7	US 20020065997		US-PGPU	20020530	22
8	US 6628551 B2		USPAT	20030930	10
9	US 6621752 B2		USPAT	20030916	9
10	US 6594196 B2		USPAT	20030715	21
11	US 6549451 B2		USPAT	20030415	11
12	US 6510098 B1		USPAT	20030121	12
13	US 6510075 B2		USPAT	20030121	11
14	US 6487107 B1		USPAT	20021126	5
15	US 6469925 B1		USPAT	20021022	6
16	US 6288952 B1		USPAT	20010911	9
17	US 6256256 B1		USPAT	20010703	19
18	US 6094378 A		USPAT	20000725	9
19	US 5923610 A		USPAT	19990713	12
20	US 5923593 A		USPAT	19990713	14
21	US 4819209 A		USPAT	19890404	20

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a cache memory coupled to said first and second ports, wherein during a read operation subject to one of said memory cells through one of said first and second ports a data stored in said one of said memory cells is read out from said cache memory if it is determined that said cache memory contains said data stored in said one of said memory cells; and

a refresh control circuit performing a refresh of the information stored within said memory cells, said refresh control circuit refreshing memory cells through one of said ports while reading data out of said cache memory.

2. The IC according to claim 1, wherein said cache memory comprises a tag portion, an address portion, and a data portion corresponding to each other, wherein said tag portion indicates if said corresponding address and data portions contain valid address and data values.

3. The IC according to claim 2, wherein said first and second ports each comprises an address path and a data read path, said address paths of said first and second ports being connected to said address portion of said cache memory and said data read paths of said first and second ports being connected to said data portion.

4. The IC according to claim 3, wherein said cache memory comprises an address comparator which is coupled to said address path of at least one of said first and second ports.

5. The IC according to claim 4, wherein said address comparator is designed to compare an address being provided through said at least one of said ports and an address being provided from said address portion of said address memory, and in case of a match designed to output the data stored in the corresponding memory cell onto the read path of said at least one port.

6. The IC according to claim 5, wherein in case of said match of addresses a refresh for a row of memory cells within the memory cell array is performed through the second port.

7. The IC according to claim 6, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.

8. The IC according to claim 7, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.

9. The IC according to claim 5, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.

10. The IC according to claim 9, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.

11. The IC according to claim 1, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.

12. The IC according to claim 11, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.

13. An IC comprising:

a memory cell array having a plurality of dynamic memory cells;

a first port and a second port for performing an access to at least one of said memory cells;

a refresh control circuit to perform a refresh for said memory cells once within a retention time interval;

a cache memory connected to at least one of said ports;

a switching device coupled to said at least one of said ports, said cache memory, and said memory cell array; and

said switching device being operated to connect either one of said memory cell array and said cache memory to said at least one of said ports in response to a read operation.

14. The IC according to claim 13, wherein said refresh control circuit performs a refresh operation while a read operation is performed through said at least one of said ports from said cache memory.

15. The IC according to claim 13, wherein said cache memory comprises a tag portion, an address portion, and a data portion corresponding to each other, wherein said tag portion indicates if said address and data portions contain valid address and data values.

16. The IC according to claim 13, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.

17. A IC comprising:

a memory cell array;

a first and a second port coupled to each one of said memory cells;

a cache memory coupled to said first and second ports;

said first and second ports comprising address terminals and data terminals; and

said second port being controlled by a refresh control circuit to perform a refresh of said memory cells.

18. The IC according to claim 17, wherein a refresh operation is performed for a row of memory cells through said second port, and a read command received through said second port is performed through said cache memory in parallel to said refresh operation.

19. The IC according to claim 17, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.

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Arial 12

[54] **MULTI-PORT DRAM CELL AND MEMORY SYSTEM USING SAME**

[75] Inventors: Fu-Chieh Hsu, Saratoga; Winnie Leung, Cupertino, both of Calif.

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Primary Examiner—Son Mai

Attorney, Agent, or Firm—Skjerven, Morrill MacPherson, Franklin & Friel LLP; Norman R. Klivans

[57] **ABSTRACT**

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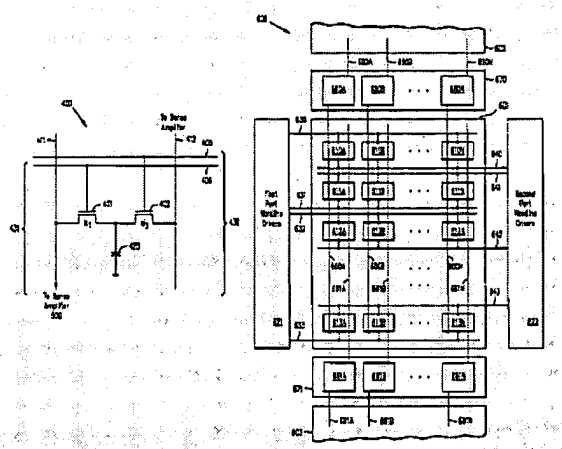

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